In re Patent Application of
ERRATICO
Serial No. **09/899,573**
Filed: **07/05/2001**
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In the Specification:

Please replace the paragraph beginning at page 15, line 11, with the following rewritten paragraph:

--Moreover, during a final step, a metal layer ~~118~~ 218 (e.g., aluminum) is formed, which is arranged on the bottom surface of the substrate 101. This metal layer 218 acts as a collector electrode for the PNP bipolar transistor of the region 205. The bipolar transistor formed in the region 205 may, for example, be a transistor for an analog (signal processing) part, while the DMOS transistor may be used as a power transistor suitable for supplying an inductive load (not shown) connected to its drain electrode D 216. This drain electrode may otherwise be placed in bias conditions which could result in the formation of an NPN parasitic transistor (including the region 104, the epitaxial layer 102, and the region 105) if the isolating element 107 were not present.--